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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,127	01/30/2004	Ping Mei	200209576-1	8740

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EXAMINER	
TRAN, THANH Y	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 01/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,127	MEI, PING	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,13-20,22 and 23* is/are pending in the application.

4a) Of the above claim(s) *11,12,21 and 24-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,13-20,22 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/30/04 & 10/3/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's election without traverse of Group I, Species I (claims 1-10, 13-20, 22-23) in the reply filed on 11/1/05 is acknowledged.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 5-6, 9-10, 13, 15-16, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Hasegawa et al (U.S 2004/0023162).

As to claim 1, Hasegawa et al discloses in figures 10A-10L a method for forming a semiconductor device comprising: forming a 3-dimensional (3D) pattern ("resist" 702) in a substrate (1001); and depositing at least one material (material of layer 1002) over the substrate (1001) in accordance with desired characteristics of the semiconductor device.

As to claim 2, Hasegawa et al discloses in figures 10A-10F a method for forming a semiconductor device, wherein forming the 3D pattern ("resist" 702) further comprises: depositing a layer (1002) of material onto the substrate (1001); imprinting a 3D pattern (702) into the layer (1002) of material; and transferring the 3D pattern (702) into the substrate (1001) (see [0045]).

As to claim 5, Hasegawa et al discloses in figures 10A-10F a method for forming a semiconductor device, wherein imprinting a 3D pattern (702) into the layer (1002) of material

(see [0045]) further comprises utilizing a 3D stamping tool ("stamper") to create the 3D pattern (702) (see [0049]).

As to claim 6, Hasegawa et al discloses in figures 10A-10F a method for forming a semiconductor device, wherein imprinting a 3D pattern (702) into the layer (1002) of material further comprises utilizing a molding process (3D pattern can be molded by a "stamper", see [0049]) to imprint the 3D pattern (702) into the layer (1002) of material.

As to claim 9, Hasegawa et al discloses in figures 10A-10F a method for forming a semiconductor device, wherein transferring the 3D pattern (702) into the substrate (1001) includes: removing a portion of the layer (first portion of layer 1002) of material thereby exposing a portion of the substrate; etching the exposed portion of the substrate (see [0050]); removing another portion of the layer of material (second portion of layer 1002) thereby exposing a second portion of the substrate; etching the second portion of the substrate (see [0050]); and removing a remaining portion of the layer (1002) of material (see figure 10D).

As to claim 10, Hasegawa et al discloses in figures 10A-10F a method for forming a semiconductor device, wherein depositing at least one material (material of layer 1002) over the substrate (1001) further comprises: depositing two sets of conductors (1003, 1004) (Figs. 10A, 10G) with a semiconductor layer (semiconductor layer of substrate 1001) a there between to form row and column electrodes overlaid in such a manner that each of the row electrodes intersects each of the column electrodes at exactly one place.

As to claim 13, Hasegawa et al discloses in figures 10A-10F a system for forming a semiconductor device comprising: means for forming a pattern ("resist" 702) in a substrate (1001) wherein the pattern (702) is 3-dimensional; and means for depositing at least one

semiconductor material (1002) over the substrate (1001) in accordance with desired characteristics of the semiconductor device.

As to claim 15, Hasegawa et al discloses in figures 10A-10F a system for forming a semiconductor device, wherein the means for forming the pattern (702) further comprises: means for depositing a layer (1002) of material onto the substrate (1001); means for imprinting a 3D pattern (702) onto the layer (1002) of material (see [0045]); and means for transferring the 3D pattern (702) into the substrate (1001).

As to claim 16, Hasegawa et al discloses in figures 10A-10F a system for forming a semiconductor device, wherein the means for depositing at least one semiconductor material (material of layer 1002) over the substrate (1001) further comprises: means for depositing two sets of conductors (1003, 1004) (Figs. 10A, 10G) with a semiconductor layer (semiconductor layer of substrate 1001) there between to form row and column electrodes overlaid in such a manner that each of the row electrodes intersects each of the column electrodes at exactly one place.

As to claim 18, Hasegawa et al discloses in figures 10A-10F a system for forming a semiconductor device, wherein the means for imprinting a 3D pattern into the layer of material further comprises means for implementing a molding process (3D pattern can be molded by a "stamper", see [0049]) to imprint the 3D pattern (702) into the layer (1002) of material.

As to claim 19, Hasegawa et al discloses in figures 10A-10F a system for forming a semiconductor device, wherein the means for transferring the 3D pattern (702) into the substrate (1001) includes: means for removing a portion of the layer of material (first portion of layer 1002) thereby exposing a portion of the substrate; means for etching the exposed portion of the

substrate (see [0050]); means for removing another portion of the layer of material (second portion of layer 1002) thereby exposing a second portion of the substrate; means for etching the second portion of the substrate (see [0050]); and means for removing a remaining portion of the layer (1002) of material (see figure 10D).

As to claim 20, Hasegawa et al discloses in figures 10A-10F a system for forming a semiconductor device, wherein the means for imprinting a 3D pattern (702) onto the layer (1002) of material further comprises means for utilizing a 3D stamping tool ("stamper") to create the 3D pattern (702) (see [0049]).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-4,14 and 17, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al (U.S 2004/0023162) in view of Ema et al (U.S. 6,664,174).

As to claims 3 and 14, Hasegawa et al does not disclose the semiconductor device comprises a cross-point memory array.

Ema et al discloses in col. 4, lines 24-33 a semiconductor device comprising a cross-point memory array ("memory cells"). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hasegawa by having a cross-point memory array as taught by Ema for storing data or "bit line" for device (see col. 4, lines 24-33 in Ema et al).

As to claims 4 and 17, Hasegawa et al does not disclose the semiconductor device is at least one of a transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse.

Ema et al discloses in figure 11A the semiconductor device is a fuse (202). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hasegawa et al by having a semiconductor device which is a fuse as taught by Ema for increasing integration of semiconductor device (see col. 2, lines 55-61 in Ema et al).

5. Claims 7-8 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al (U.S 2004/0023162).

As to claims 7, 8, 22 and 23, Hasegawa et al does not disclose the layer of material comprises a polymer material or a photo-resist material. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hasegawa et al by using polymer material or a photo-resist material for the layer of material for reducing production cost and easily depositing in the semiconductor device, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended used as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

Zandra V. Smith
Supervisory Patent Examiner
23 Jan. 2006